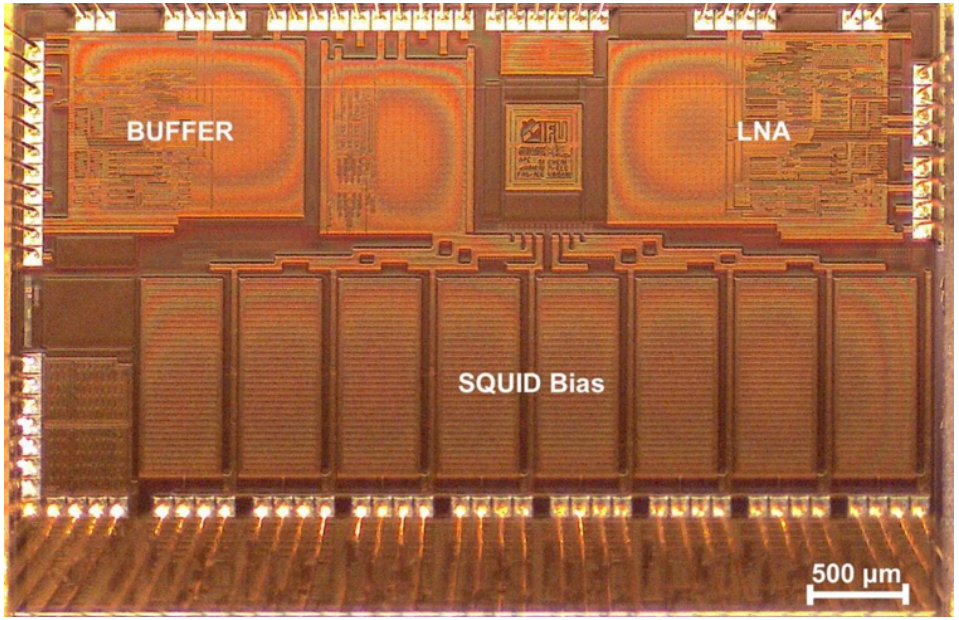
Specific Integrated Circuit for the X-IFU Warm Front-End Electronics

Damien Prêle (APC, Paris) on behalf of the WFEE and X-IFU detection chain team.

The X-IFU (X-ray Integral Field Unit) instrument of the Athena mission is designed to operate with 3168 superconducting microcalorimeters (read out by Transition Edge Sensors - TES) cooled to 50 mK, providing an imaging spectrometer for X-ray astronomy. The unprecedented spectral resolution of 2.5 eV up to 7 keV requires low noise readout electronics. Located immediately outside the cryostat, the Warm Front End Electronics (WFEE) is a key component of the readout electronics.

The WFEE amplifies the detection chain signal, adjusts the operating points of the cryogenic devices (Superconducting QUantum Interference Devices - SQUIDs), and feeds through the TES bias and feedback loop. Using Frequency Domain Multiplexing (FDM, see Athena Nugget #25 for more details), 40 microcalorimeters are read out per channel and 40 carriers between 1 to 5 MHz are injected to 40 sensors. As a result, the detected X-ray pulses are transposed into 40 different frequencies. Ultimately, about one hundred channels are needed for the full readout of the TES array.

To meet the energy resolution of the cryogenic sensors, the WFEE, like the whole readout chain, has to exhibit ultra-low noise and extremely small gain-drift. At the same time, the size, the mass, and the dissipation must be minimized as required for a space mission. For this reason, an Application-Specific Integrated Circuit (ASIC) has been designed for the WFEE. "350 nm BiCMOS SiGe" ASIC technology is used for the core of the WFEE. "350nm" corresponds to the minimum gate size of MOS transistors. "BiCMOS" means that both bipolar transistors and complementary (N and P) MOS transistors can be built using this technology. Finally, "SiGe" indicates that Silicon-Germanium alloy is used to make the base-emitter junction of the bipolar transistor. Such a hetero-junction increases the speed of the transistors allowing the design of a wide-band amplifier covering the frequency range of the carriers used for the FDM. The micro-photograph illustrates an ASIC chip design for the WFEE. Eight independent readout channels will be integrated on a chip of one square centimetre.



Micro-photograph of one WFEE readout channel in an integrated circuit: AwaXe_ v2.5. The figure shows the LNA (Low Noise Amplifier) to amplify the multiplexed signal; the Buffer to drive the biasing of the sensors; and finally four differential quasi-DC SQUID Bias with associated bus decoders to adjust the operating points of the readout chain.Credit: Damien Prêle.

The noise degradation of WFEE is minimized by reducing any parasitic resistance and thanks to fine-tuning of the transistors biasing to operate in an optimal noise condition.

The gain drift is also a significant contributor to the energy resolution budget. At large time scale (> 1s), the thermal drift is the main cause of electronic parameter shifts. The entire circuit is based on a specific design including thermal compensation techniques.

The WFEE with its custom designed ASIC is a compact, light-weight component with minimal power consumption and it delivers the high performance required for Athena's X-IFU readout electronics.