Fast onboard data preprocessing for the Athena Wide Field Imager (WFI)

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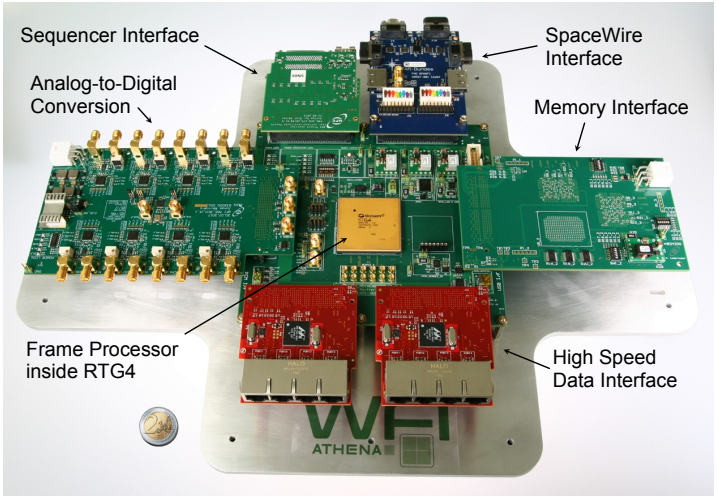
The focal plane of the WFI instrument onboard *Athena* consists of two detectors that feature a large number of pixels, which are read out at an extraordinary high rate: The Large Detector Array is a 1,024 x 1,024 DEPFET matrix composed of four 512 x 512 pixel quadrants which are operated at 200 frames/s while the Fast Detector has only 64 x 64 pixels but is recording at an impressive rate of 12,500 frames/s.

The enormous amount of data generated by these devices cannot be simply stored and transmitted to ground due to limitations on the available telemetry bandwidth. Therefore, real-time data screening and preprocessing are required directly within the detector electronics. As only a few of the pixels in each frame contain information about the observed photons from astrophysical sources, it is possible to identify relevant pixels and transmit only their information.



Frameprocessor breadboard prototype - RTG4 motherboard incl. peripherals. Credit: WFI team.

This task is performed by the WFI Frameprocessor (FP), a digital electronics design written in the Hardware Description Language VHDL and synthesized into a single chip. An FP performs the event data preprocessing (EPP) for the fast detector (or for one of the 512 x 512 pixel quadrants of the large detector). In addition, it also contains a programmable memory sequencer that will generate all control signals necessary to operate and configure the readout chips as well as the Analog-to-Digital Converters.

The preprocessing consists of an offset correction per pixel, a common mode correction, programmable event energy thresholds and several event flagging tasks to identify pixels that are part of ionising particle tracks. Some of the tasks are performed on a pixel individual basis, others seamless on the whole detector quadrant, like the pattern recognition that is applied to identify only single-photon event pixel patterns or the flagging of pixels close to particle tracks. The EPP is also able to generate, process and store the data of the pixel lookup tables needed for offset correction and energy threshold detection during calibration.

The output of the FP will provide the data in an event list format typically used for X-ray observatories via a SpaceWire Interface Controller.

The current VHDL design of the FP has been tested on a Xilinx Virtex-5 FPGA as well as on the radiation hard Microsemi RTG4 FPGA. It will typically operate at a clock frequency of 80 MHz where it can process input data rates of up to 3 Gbit/s which would correspond to a rate of 800 frames/s for the large detector. The output data rate that the FP is able to sustain is directly related to the number of photons seen by the detector and can vary from 0 to as high as 2000 events/frame in each quadrant.

The development of the Frameprocessor firmware is carried out by the Institute for Astronomy and Astrophysics in Tübingen in close collaboration with the Max Planck Institute for Extraterrestrial Physics in Garching, where a prototype of the Detector Electronics is being developed and tested.